Amendments to the Specification

Please replace the paragraph starting on page 10, line 29 through page 11, line 19 with the following rewritten paragraph:

The reconfigurable memory controller 204 includes configuration registers which can be externally programmed in order to realign the logical addressing and map out bad memory blocks. The registers in one embodiment are externally programmed when the ~~integrated circuit~~ reconfigurable memory 102 is embedded within a system. Upon initialization, the reconfigurable memory 102 is tested and the initialization software programs the configuration registers to map out and realign the logical addressing. In another embodiment, the configuration registers are non-volatile or have a fuse-link type of programmability and can be programmed at the factory. In this case, the integrated circuit is tested in wafer or packaged form at the factory and the configuration registers are programmed as well accordingly. In either embodiment, the testing and reconfiguration of the reconfigurable memory can be transparent to the system designer and user of the printed circuit board incorporating the integrated circuit 102. The testing of the reconfigurable memory 102 can be done by the integrated circuit itself by using the BIST when in a system. Alternatively, the reconfigurable memory 102 can be externally tested by production test software through the pins of a packaged integrated circuit or the pads of a die of the integrated circuit in wafer form.

Please replace the paragraph starting on page 18, line 1 through line 13 with the following rewritten paragraph:

To reprogram the reconfigurable memory 102, software executing on an external host controller or within the integrated circuit 100 can read the pass/fail information within the test register 108 and set/clear the enable bit ~~604~~ 704 and the values of the chip select base address 706 in each configuration register 702 accordingly for each memory block 212. The values of the chip select base address 706, the most significant address

bits, set by the external host controller can linearize the logical addressing by setting a linear sequence of 0, 1, 2, 3 and so on, incrementing by one. Alternatively, a different logical addressing scheme can be utilized by programming the values of the chip select base address 706 differently.

Please replace the paragraph starting on page 19, line 3 through line 16 with the following rewritten paragraph:

Each enable bit 704 in each configuration register 702 controls whether or not the respective memory block 212 is to be mapped out or not. If the enable bit 704 is set, the respective memory block 212 is not mapped out. If the enable bit 704 is not set, the respective memory block 212~~+~~ is mapped out. The enable bit 704 gates the generation of the chip select signal 216n. If the enable bit 704 is set, the chip select signal 216n can be generated through the AND gate 804 if the upper addresses match the chip select base address. In this case, the respective memory block 212 is not mapped out. If the enable bit 704 is not set, the chip select signal 216n can not be generated through the AND gate 804 regardless of any address value and the respective memory block 212 is mapped out.